COMP 201: Computer organization and Architecture [3 Credit]

Objectives
General principles of computer organization and aspects of design logic, including the following topics: Von Neumann machine architecture, CP and AL design, instruction set formats, addressing modes, memory systems and subsystems, I/O devices and operations.

Contents:

1. Basic Structures
   1.1. Sequential Circuits
   1.2. Design procedures
   1.3. State Table and State Diagram
   1.4. Von Neumann architecture
   1.5. Stored Program Concepts
   1.6. Functional Units

2. Addressing Methods and Programs
   2.1. Programming View of a processor
   2.2. Data types
   2.3. Representation of data
   2.4. Arithmetic operations
   2.5. Basic operational concepts
   2.6. Bus structures
   2.7. Instruction cycle
   2.8. Excitation Cycle

3. Processing Unit
   3.1. Instruction formats
   3.2. Computer instruction
   3.3. Instruction length
   3.4. Address instruction
   3.5. Arithmetic instruction
   3.6. Logical instruction

4. Addressing mode
   4.1. General concepts
   4.2. Single component addressing modes
   4.3. Multi-component addressing modes
   4.4. Position independent code

5. Input Output Organization
   5.1. Basic principles of interrupt driven I/O and DMA
   5.2. I/O operations
   5.3. I/O programming
   5.4. Memory mapped I/O
5.5. Basic Interrupt system
5.6. Direct Memory Access
5.7. DMA channel programming
5.8. Memory mapped screens

6. Arithmetic
   6.1. Magnitude comparator
   6.2. Complements
   6.3. Straight subtraction
   6.4. Subtraction with components
   6.5. Addition and subtraction algorithms
   6.6. Hardware implementation
   6.7. Multiplication and division algorithms
   6.8. Hardware implementation
   6.9. Divide overflow

7. Memory System
   7.1. Auxiliary memory
       7.1.1. Magnetic Drum
       7.1.2. Magnetic Disks
       7.1.3. Magnetic Tapes
   7.2. Micro-computers

8. Memory
   8.1. RAM/ROM chips
   8.2. Memory address map
   8.3. Memory connection to microprocessor
   8.4. Memory hierarchy
   8.5. Associative memory
       8.5.1. Hardware organization
       8.5.2. Match logic
       8.5.3. Read operation
       8.5.4. Write operation
   8.6. Virtual memory
       8.6.1. Address space
       8.6.2. Memory space
       8.6.3. Address mapping
       8.6.4. Associative memory page table
   8.7. Cache memory
       8.7.1. Associative mapping
       8.7.2. Direct mapping
       8.7.3. Set associative mapping
   8.8. Memory management hardware
**Text Books:**
Computer System Architecture – *M. Morris Mano*

**References:**
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**Evaluation:**
Internal = 50
Final = 50